

1 ABSTRACT OF THE DISCLOSURE

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3 A method and system for generating a synchronous sequence
4 of vectors from information originating within an asynchronous environment is
5 disclosed. A simulated asynchronous sequence is synchronized by extracting
6 a state at each clock period to generate a simulation synchronous sequence.
7 This sequence is manipulated first to include short delays for generating an
8 asynchronous short-delay sequence and second to include long delays for
9 generating an asynchronous long-delay sequence. An overlay is separately
10 performed among the clock periods of the asynchronous short-delay
11 sequence and the asynchronous long-delay sequence to respectively identify
12 a first interval and a second interval. The first interval and the second interval
13 are independently duplicated in successive clock periods to respectively
14 generate a synchronous short-delay sequence and a synchronous long-delay
15 sequence. An overlay is performed on the two sequences to enable
16 generation of the synchronous sequence of vectors for verifying operations of
17 an IC design by a tester.

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